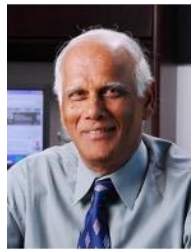
Exploring the Impact of Industry-Government Co-Investments for the Advanced Electronics Sector in North America, Asia and Europe

In an era defined by technological advancement and digital transformation, the semiconductor and microelectronics packaging industry plays an important role in shaping the global economy and innovation landscape. The introduction of the CHIPS and Science Act (Creating Helpful Incentives to Produce Semiconductors for America) in the United States. Since then other key countries and regions have outlined similar programs to invest in the microelectronics industry growth. In Europe, the European Chips Act has generated significant interest and discussion. This special session aims to dive deeper into the multifaceted opportunities offered by the CHIPS Acts, as well as their potential impact on the semiconductor and microelectronics packaging industry in North America, Europe and Asia. The speakers will address the potential economic benefits of the government led programs and co-investments for the United States, Europe, India and Japan, including job creation, supply chain resilience, and enhanced technological innovation. We will examine the prospects of global collaborations and partnerships between national semiconductor and microelectronic packaging centers and industry leaders. The panel will also discuss mechanisms for knowledge exchange, joint research initiatives, and mutually beneficial outcomes.

Dr. Elisabeth Steimetz
Europe

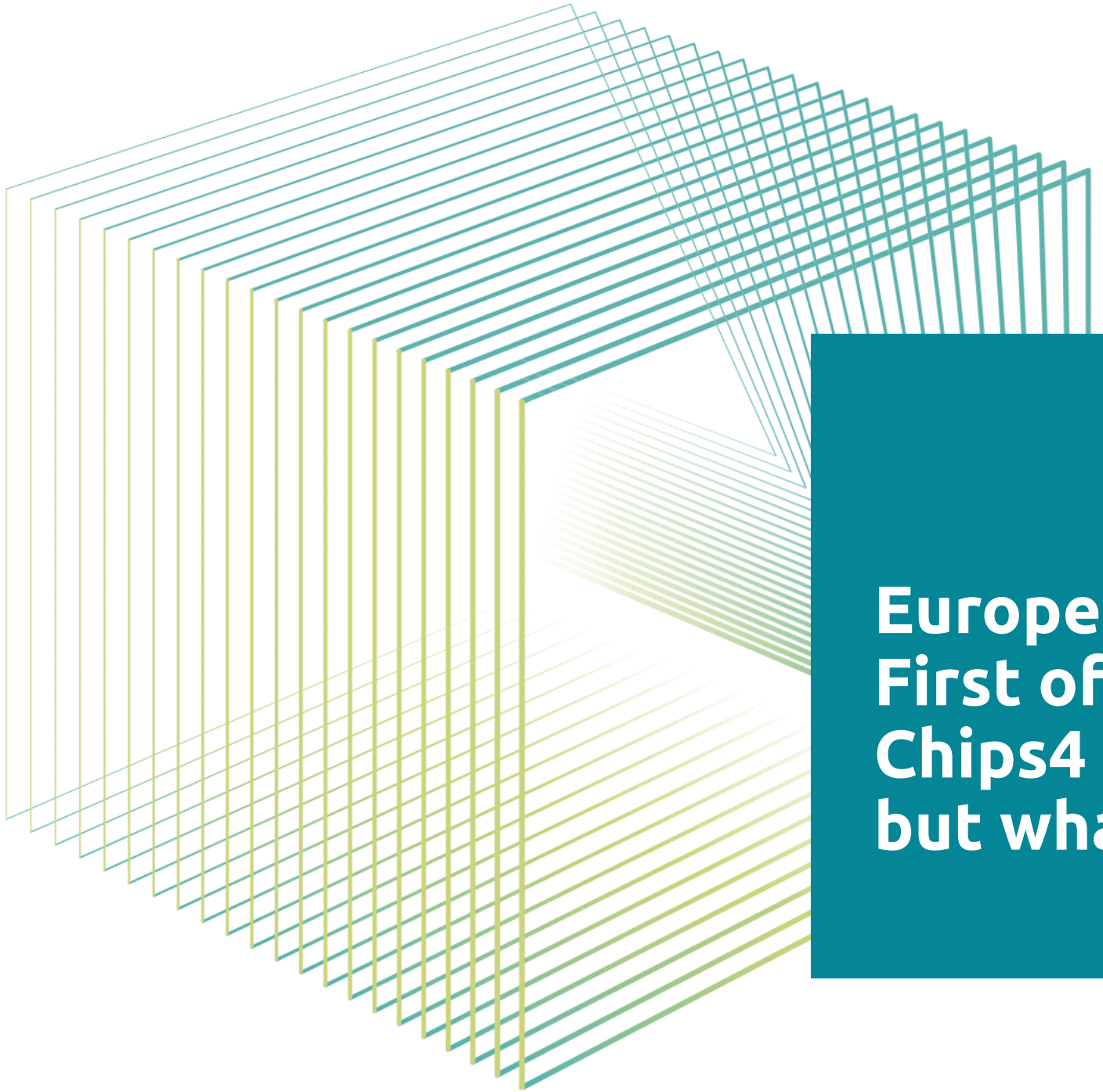


Prof. Rao Tummala
India

Dr. Eric K. Lin
USA

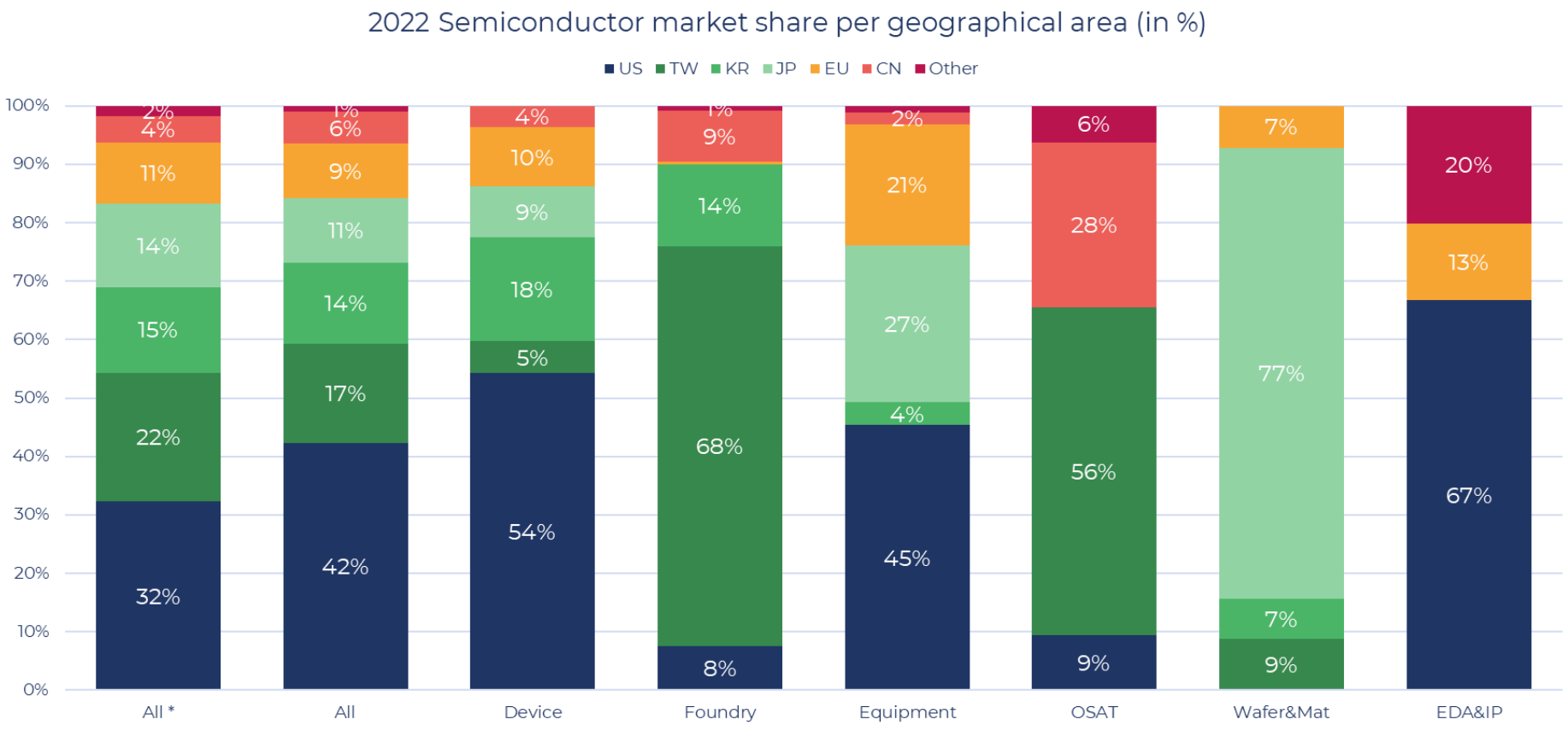
David Lynch
Canada

Dr. Kwang-Seong Choi
Korea



European Chips Act – First of a kind fabs, IPCEI and Chips4 EU initiative – but what about packaging?

2022 Semiconductor Market Share per geographical area in %



TW + CN : 84% of OSAT

JP + KR : 84% of Wafers & Material

Source: Yole

European Chips Act | Three Pillars and a whole bunch of funding instruments

I
Chips for Europe Initiative

R&D Infrastructure:
- Competence Centers
- Pilot Lines (up to TRL 4-5)
- Design platform

Support for Start-Ups und SME

II
Security of Supply

First-of-a-kind in Europe
- Production capacity
- Innovation in products and production

III
Monitoring and Crisis Response

- Analysis of value chain
- Risk coordination and monitoring
- Risk managment

European Chips Act | Pillar 1
Chips4EU initiative

Under the framework of the Chips Joint Undertaking
the new **Chips4EU Initiative (Pillar 1 of Chips Act)** will fund:

1) Research **pilot lines at RTOs** (2nm FinFet, 7nm FD-SOI, Heterogeneous Integration, Wide Bandgap, Photonics, Quantum, …)
2) A **European Design Platform**
3) Up to 26 **Competence Centers**
4) **Skills** developments

The Chips JU builds upon the former KDT JU. The total EU contribution for funding was increased from €1.8 billion to **up to €4.175 billion.**

The first 4 RTO pilot lines have been selected for funding in April, 2024, one will be on **Advanced Heterogeneous Integration.**

Our Pilot Lines · Chips Ju (europa.eu)

European Chips Act | Pillar 2
„First-of-a-kind in Europe“ investments

Approved by EC

Catania (Italy)
- Industrial SiC production
- 730 mio. € investment (292 mio. € funding)

Crolles (France)
- FD-SOI-technology (18 nm)
- 7.4 bn. € investment (2.9 bn. € funding)

Pre-notified at EC

Magdeburg (Germany)
- Advanced technology nodes
- 30 bn. € investment (10 bn. € funding)

Wroclaw (Poland)
- Fab for packaging
- 4.8 bn. € Investment

Dresden (Germany)
- „Smart Power Fab“
- 5 bn. € investment (1 bn. € funding)
- Combined IPCEI ME/CT and ECA

Dresden (Germany)
- Mature technology nodes (12-28 nm)
- 10 bn. € investment (5 bn. € funding)

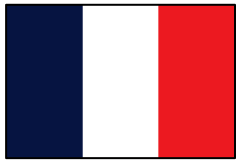
Ensdorf (Germany)
- 200 mm SiC chip production
- 2,8 bn. € investment (700 mio. € funding)
- Combined IPCEI ME/CT + ECA

2nd IPCEI on Microelectronics and communication technologies (funded by EU Member states)

IPCEI Microelectronics and Communication Technologies

In total, **99 partners** from **20 European Member States** participate in the IPCEI ME/CT:


Germany
25 projects


France
14 projects


Italy
8 projects


Austria
6 projects

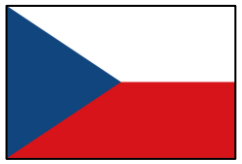

Spain
10 projects


Slovakia
4 projects

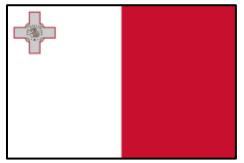

The Netherlands
3 projects


Greece
6 projects


Romania
5 projects


Czech Republic
4 projects


Ireland
1 project


Malta
1 project


Finland
1 project


Poland
1 project


Portugal
3 projects


Norway
2 projects


Slovenia
2 projects


Belgium
2 projects

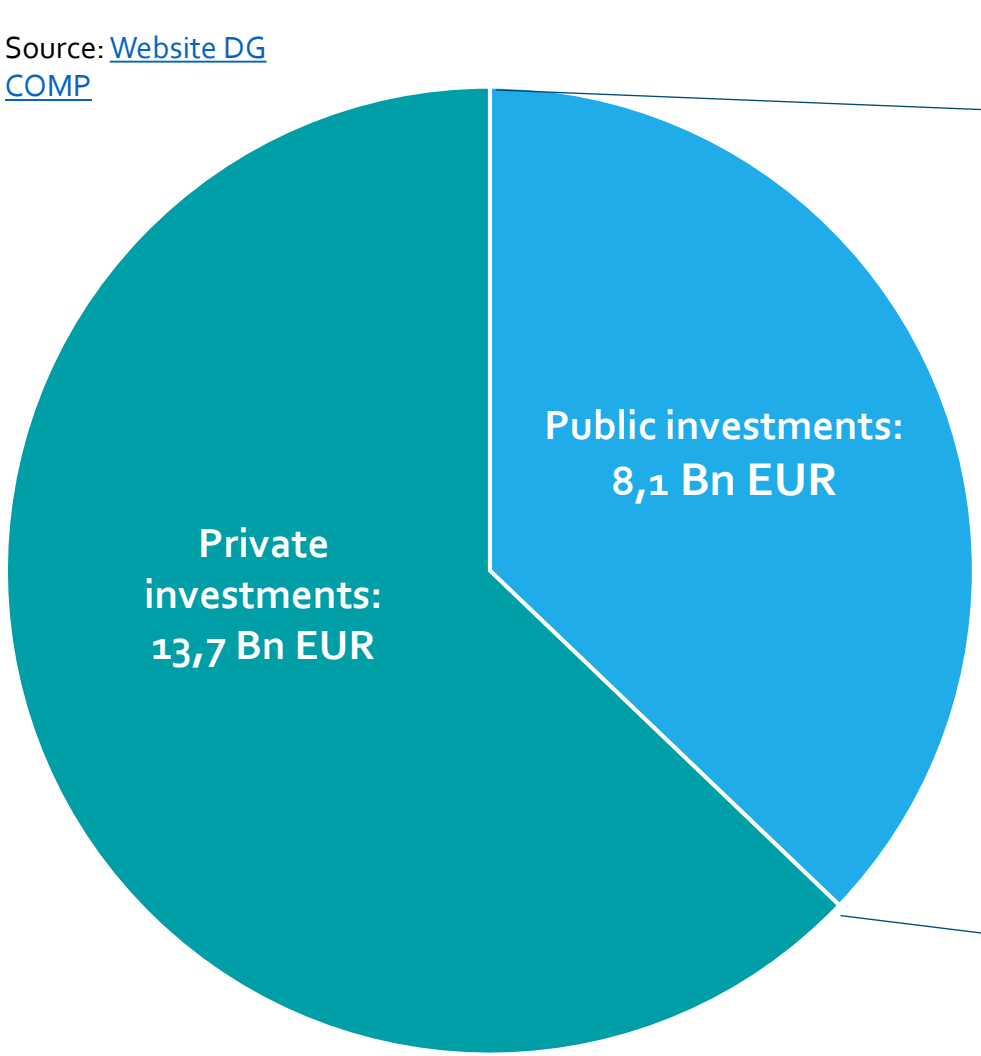

Hungary
1 project

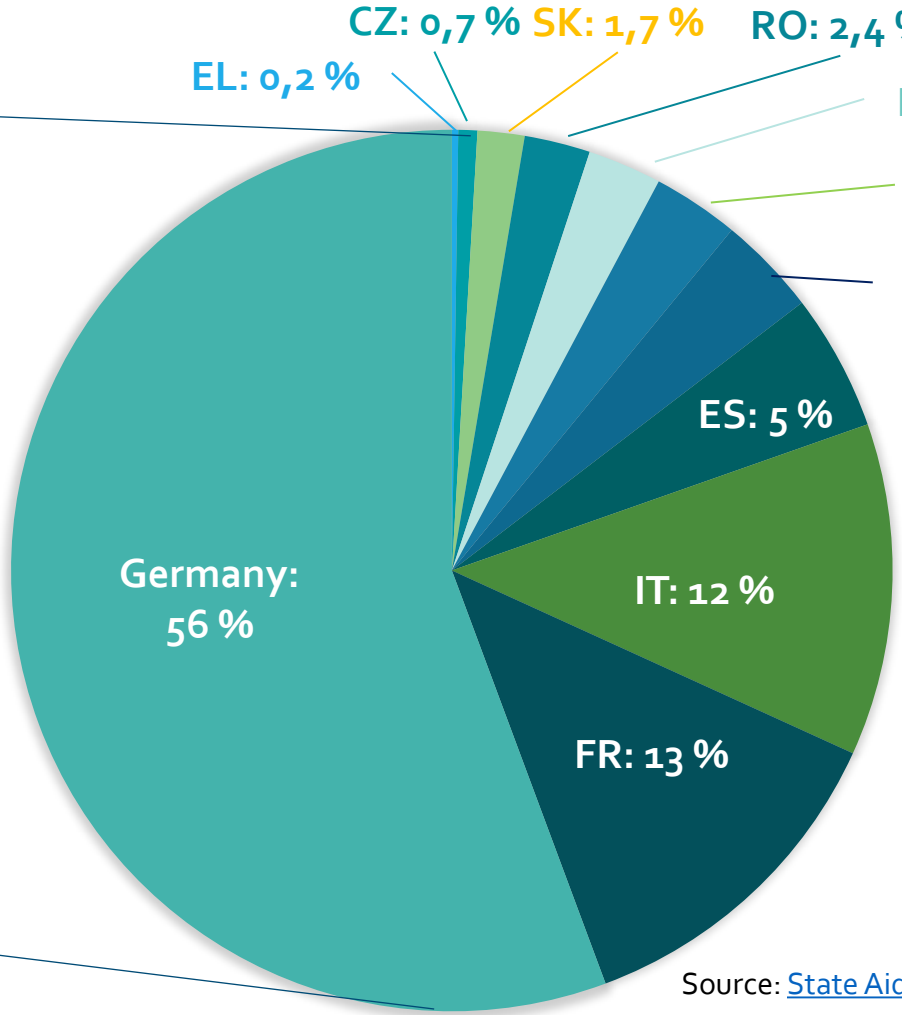

Latvia
1 project

Source of pictures: https://www.nationalflaggen.de/

IPCEI ME/CT: Planned investments

Source: Website DG COMP





Source: State Aid Decision

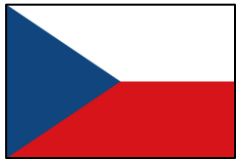
Advanced Packaging in the IPCEI ME/CT:

- The IPCEI ME/CT addresses the **entire European microelectronics value and supply chain**, from material manufacturers and suppliers to design and foundries, integrated device manufacturers (IDM), outsourced semiconductor assembly and test (OSAT) and end-users.
- In total, **22 projects** (out of 99) directly deal **with packaging and advanced packaging**. Thereby, the focus lies on development of new technologies (e.g. flip chip, wafer bonding, chiplets, system-in-package), materials (e.g. organic substrates, glass) as well as packaging and test equipment.
- The objective is to move away from the current semiconductor assembly and test services provided at large-scale, and **develop smaller, highly flexible advanced packaging services in Europe**, which would help European players to implement and test even small volumes and innovative solutions.

Further Announcements about planned investments in Europe

- March 2024: 3.2 bn. € investment for Silicon Box (focus: chiplet technology)
- May 2024: 10 bn. € investment in national chip capacity announced

- April 2024: Launch of a new state-owned technology investment company with a capital of 20 bn. €



- April 2024: TSMC announced to establish an IC design education center in Prague

The Chips Act helped to create awareness for the importance of the semiconductor industry in and for Europe
and stimulated investments by many countries and regions across Europe!

How about packaging?

PACK4EU

CSA **Pack4EU:**

Objectives: Creation of a
Pan-European network for Advanced packaging
and a Roadmap to **boost packaging** in and for Europe

Consortium:

BLUMORPHO, cea, High Tech NL, VDI|VDE|IT, semi, iMAPS, TU Delft

Core objectives are to **assess the current status** and to **analyze the evolving needs** of the semiconductor industry regarding **advanced packaging, assembly and test in Europe** by mapping existing facilities, evaluating technological capabilities and identifying areas for improvement.

June,12 the project will present its final recommendations to the European commission.
Final Event: June, 18 2024
For further information and regular up-dates: Pack4EU: Beiträge | LinkedIn

To the survey:

International Cooperation On Semiconductors

OUTCOME & IMPACT

- **Raise awareness of the advanced research activities** inside and outside Europe
- **Reduction of the gaps & Increase European Leadership** in Semiconductor & Semiconductor-based photonics
- **Facilitate the European industry in the realization of emerging technologies**: advanced computation & advanced functionalities
- **Reinforce the position of the European industry** through new standards
- **Contribute to the European Strategic Autonomy** through balanced partnership with like-minded leading countries
- Contribute to other European initiatives in this sector : **European Chips Act & Digital Agenda.**
- **Contribute to the realization of the Green Deal:**
  - Digitalisation of many domains to reduce footprint
  - Electronics monitoring targeting societal challenges (energy, health, environment, etc.)
  - Sustainable electronics (energy consumption, critical materials, etc)

PARTNERS

ACADEMICS

RTOS

INDUSTRIAL ADVISORY BOARD

Robert Chau, Director Intel Europe Research
Paolo Azzoni, Inside General Secretary
Laith Altimime, President
Elisabeth Steimetz, Director
Carlos Lee, Director
Colin Willcock, Chairman of the Board

ASSOCIATIONS & CONSULTING COMPANIES

INDUSTRIALS

INTERNATIONAL ADVISORY BOARD

Ray, Jui-Lin Yang, Head of Semiconductor Research Dep.
Jose Pozo, Chief technology officer
Hayashi Yoshihiro, Chairman
Paolo Gargini, Chairman

Chips JU launched a first call with **South Korea** for common R&D&I in the area of neuromorphic computing
and **heterogeneous integration** (6 Mio. EUR EU funding)

Further calls with other countries are under preparation;

Summary

- The **European Chips Act** has enabled huge investments in first-of-a-kind Fabs in Europe. A second **IPCEI** started with 99 partners across Europe.
- **Investments in RTO pilot lines** and a European **design platform** under the Chips4EU initiative will follow soon.
- The **Pack4EU** initiative started last summer to create a Pan European Network for Advanced packaging. But advanced packaging is not yet in the focus of the activities in Europe!
- An action plan to **accelerate the Lab-to-fab transfer** from RTOs into industry in Europe and the set-up of local **open industrial manufacturing sides** for advanced packages for critical European markets (low and mid-size volumes) have to follow.
- Europe cannot act alone! We need **international collaboration** for a sustainable growth of our semiconductor and other industries (not only automotive).
- International R&D programmes are needed and strategic alliances.

A “NATO of Chips & Adv. packaging” has been proposed by somebody lately –

food for thought and discussion!

Greetings from Indian Semiconductor Mission

India's Chips Act

- $10B for Manufacturing
- >$ 1B for Technology Development & Pilot Lines
- $0.5B for Research (5 Years)

Prof. Rao R. Tummala

Advisor to Government of India

- **Emeritus Professor and Founding Director, Georgia Tech PRC**
- **IBM Fellow & Director of Packaging, IBM**

इंडिया सेमीकंडक्टर मिशन
India Semiconductor Mission

Indian DSPS R&D Team. Together, We Can.

Emergence of India as a Semiconductor Nation

- 3rd Largest Economy by 2030
- Fastest Growing G20 Economy
- 2nd Largest Internet User
- Largest AI Tools User
- 3rd Largest Start-Up System
- 33M Graduates

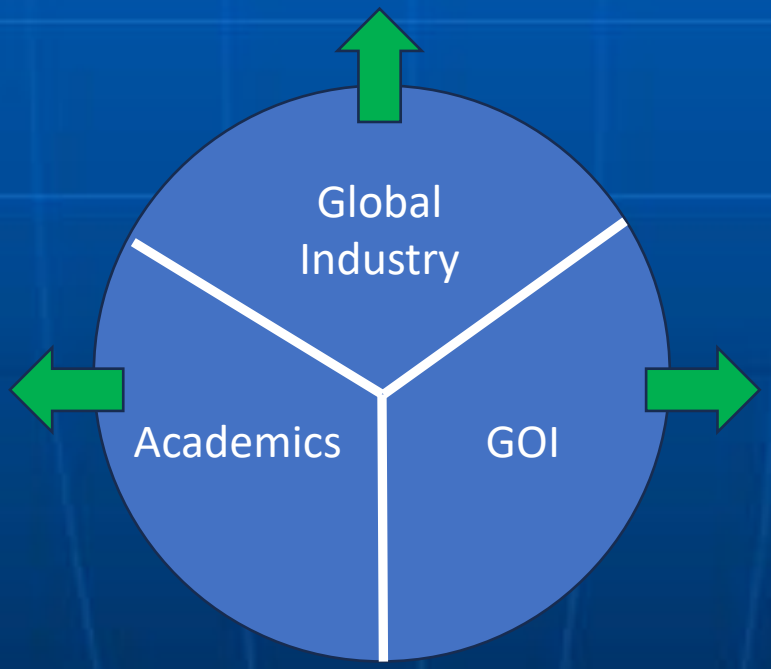
India Has All Except Technology & Mfg. Infrastructure, Expertise and Resources

Competitive Factor	Strengths/Weaknesses
Market Size	
Educated Workforce in Basic Sciences & Engineering	
Design Expertise & Resources	
R&D Infrastructure, Expertise & Resources	
Manufacturing Infrastructure, Expertise & Resources	
Investment Opportunities in R&D	
Investment Opportunities in Manufacturing	

Strong Fair Weak

India as A Global Hub by Three Way Partnership- Academics-Industry-Government

- Invest in Mini COEs as Spokes with CSR Funds
- Fund R&D Projects
- Assign Industry Engineers on Campus For SRA D&Ds
- Work with ISRC for integrated Industry Prototypes

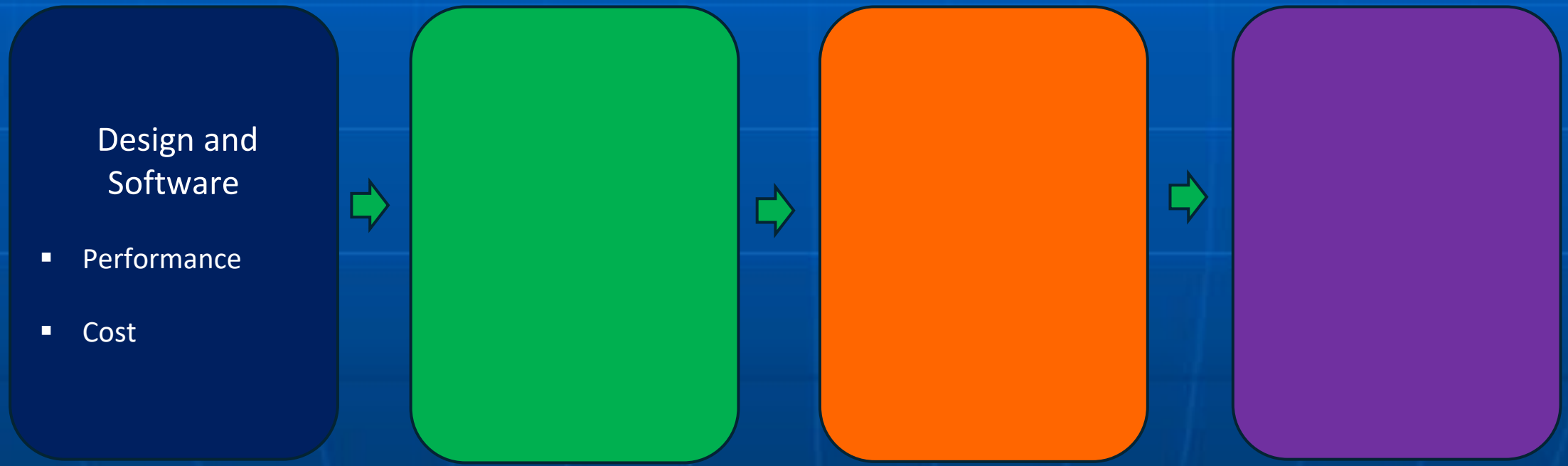


- Set-Up Industry-Centric COEs for R&D and Workforce Development
- Adopt Industry-Centric Culture
  - Industry Engineers on Campus
  - Industry Prototypes
- Recognize & Reward Faculty & Students

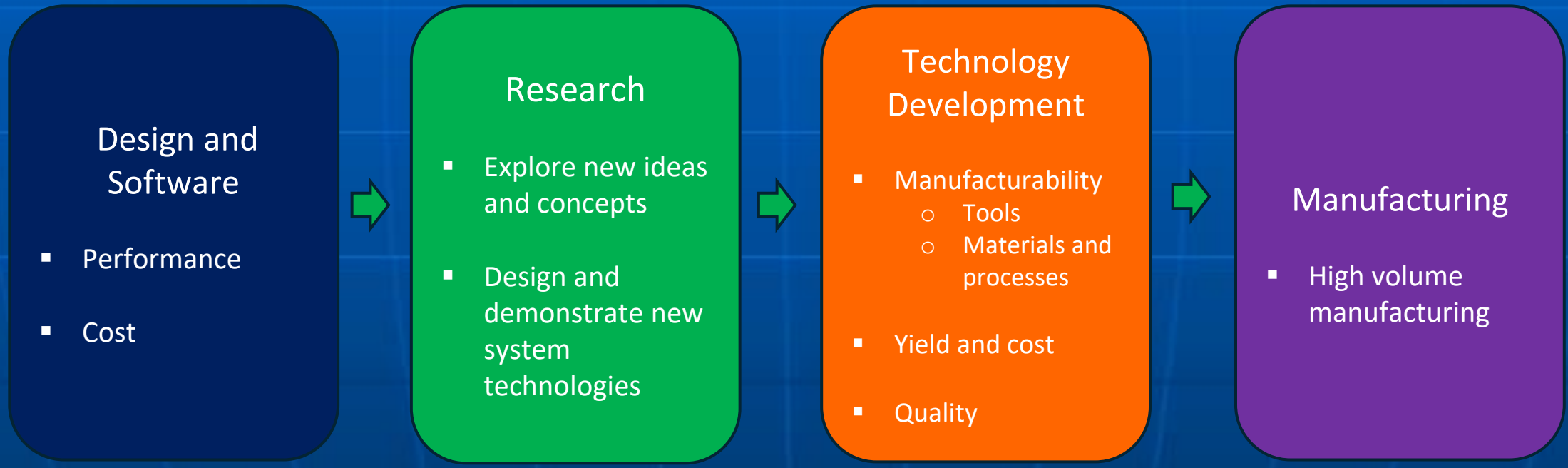
Invest in R&D & Workforce Infrastructure for 12 SRAs

- Set-Up Industry- Driven Management System
- Fund 50/50 for R&D and 100% for Education

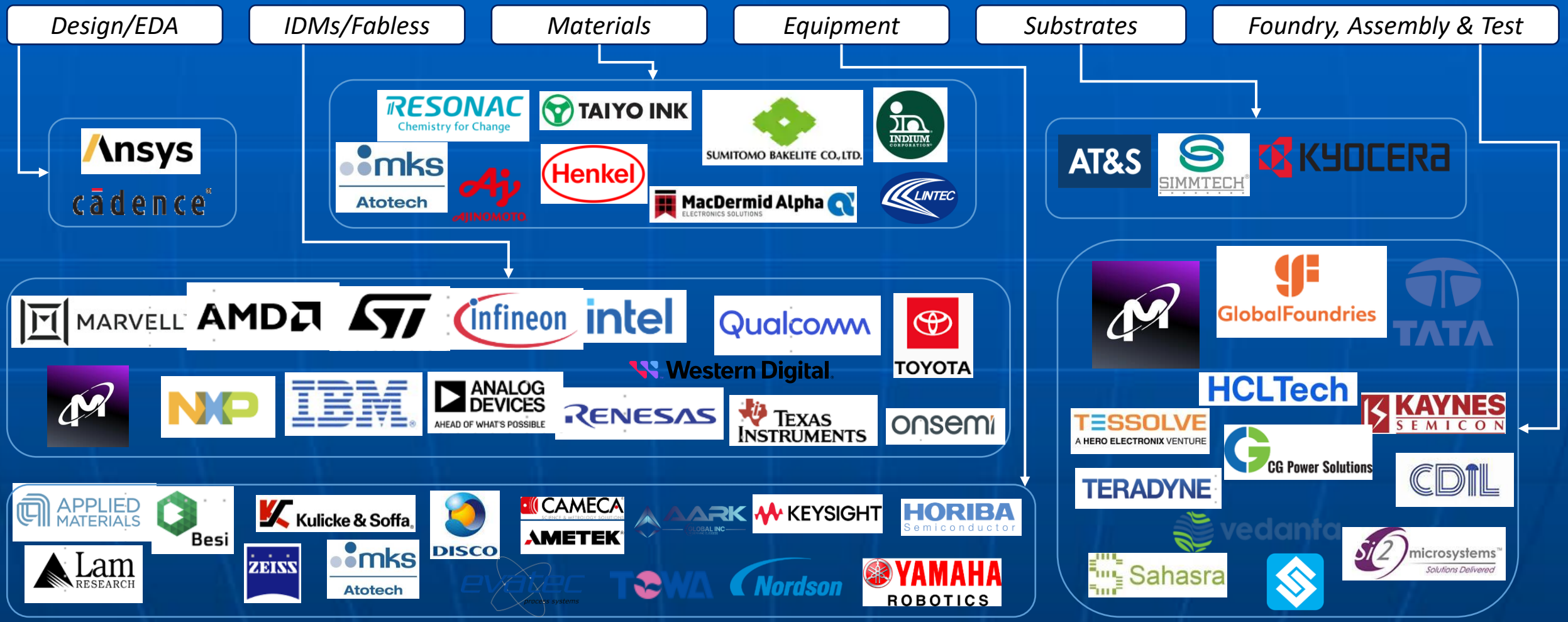
India has Design and Software Only Now But All in Near Future



India has Design and Software Only Now But All in Near Future



Semiconductor & Packaging Global Supply Chain for R&D & Mfg. in India



- Creation of an Indian semiconductor & packaging supply chain and investments are well underway
- Many more Indian companies are interested in R&D + manufacturing and attending ISPEC 2024

Global Companies and Global Collaborating Centers for R&D Industry Consortium

ISM Participating Companies

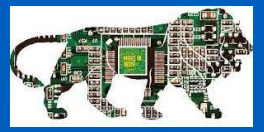
Global R&D Centers

Potential Global Academic Collaborators

SRA – Devices		SRA – Power Electronics		SRA – Thermal Technologies		SRA – Substrates	
Saptarshi Das *Penn State*	Kaushik Roy *Purdue*	Alan Mantooth *Univ. of Arkansas*	Vanessa Smet *Georgia Tech.*	Satish Kumar *Georgia Tech.*	Justin Weibel *Purdue*	Venky Sundaram *Georgia Tech.*	Pratik Nimbalkar *Georgia Tech.*
							

SRA – Co-packaged Optics		SRA – Predictive Modeling		SRA – 6G		SRA – IC and Board Assembly	
Stephen Ralph *Georgia Tech.*	Ajay Jacob *Univ. of S Calif.*	Abhijit Dasgupta *Univ. of Maryland*	G. Subbarayan *Purdue*	M. Swaminathan *Penn State*	Aritra Banerjee *Univ. of Ill. Chic.*	Shubhra Bansal *Purdue*	Vanessa Smet *Georgia Tech.*
							

SRA – Materials		SRA – System Des. & Architec.		SRA – MEMS and Sensors	SRA – Electrical Test
Suman Dutta *Georgia Tech.*	Kaushik Roy *Purdue*	A. Raghunathan *Purdue*	V. Raghunathan *Purdue*	Sunil Bhave *Purdue*	Abhijit Chatterjee *Georgia Tech.*
					



2nd Indian Semiconductor and Packaging Ecosystem Conference (ISPEC)
March 6-8, 2025, Gandhinagar, Gujarat, India

Purpose of the Conference: As India enters semiconductor and package manufacturing with $10B incentives from ISM, India needs to develop the entire ecosystem from design to R&D to manufacturing, products, applications and services as well as workforce development. This ecosystem requires researchers, developers, suppliers for materials and tools as well as manufacturers and users. This is the purpose of the 2nd Indian Semiconductor and Packaging Ecosystem Conference (ISPEC) with a focus on global level R&D and workforce development in partnership with global industry, leading to a large-scale industry–academic consortium in next generation of semiconductors, packaging and systems in India.

Technical Focus: The focus of strategic R&D in India is in integrated semiconductors and systems packaging for such emerging large-scale product sectors as computing and AI, 6G and beyond communications, ultra-high-power modules for electric cars and integrated sensors for IoT and medical electronics. Such product sectors require next gen, global level R&D, education and skill development and global industry partnerships spanning from system design and 3D architectures to devices to interconnecting electronic and photonic substrates to solderless Cu to Cu assembly, predictive modeling and design, thermal management and integration of all these into 3D Chiplet logic-memory modules, 6G Integrated 3D antenna-in package, 3D integrated power modules and 3D energy efficient and miniaturized mems and sensor modules and advances in system level electrical test.

Attendees: The conference brings global R&D, suppliers , manufacturers, and users from US, Europe, Japan, Korea, Taiwan and India. The expected attendees include global and domestic industry executives and technical leaders as well Indian and global faculty and students. A total of about 500 attendees are expected for the 2nd conference.

Executive Committee

Industry	Advisor(s)
TBD	TBD
TBD	TBD
TBD	TBD

General Chairs

Affiliation	Advisor(s)
Georgia Tech	Prof. Rao Tummala
IESA	Ashok Chandak
Gandhinagar	Nihar Mahopatra
IEEE EPS Meity	TBD

Technical Chairs

Affiliation	Advisor(s)
Industry	TBD
IEEE EPS	TBD
Academic	Nilesh Badwe

Conference Organizers

Function	Advisor(s)
Website	
Registration	
Hotel & Airport Pick-Up	
Venue and Food	
Budget	

Day 1: March 6: Inaugural and Executive Sessions

1. Inaugural Session: Ashok Chandak, IESA and Prof. Moona, IITGN
2. Plenary Sessions:
   a) Industry Keynote Session: Dr. Charan Gurumurthy, Tata, and Dr. Hern Takiar, Micron
   b) Academic Keynote Session: Prof. Dasgupta and Prof. Swaminathan
   c) Director's Session: Prof. Ramgopal, VC, BITS, Pilani and Prof. Rao Tummala, Georgia Tech

Day 2: March 7: R&D, COEs and Industry Consortium Sessions

1. R&D, COEs and Industry Consortium in 12 SRAs: Prof. Rao Tummala and Dr. Ravi Mahajan
2. Student Poster Session: Prof. Nilesh Badwe, IITK and Dr. Arun Chandrasekhar, Intel
3. Industry Consortium: Strategy, Status & Plans: Prof. Rao Tummala, Georgia Tech

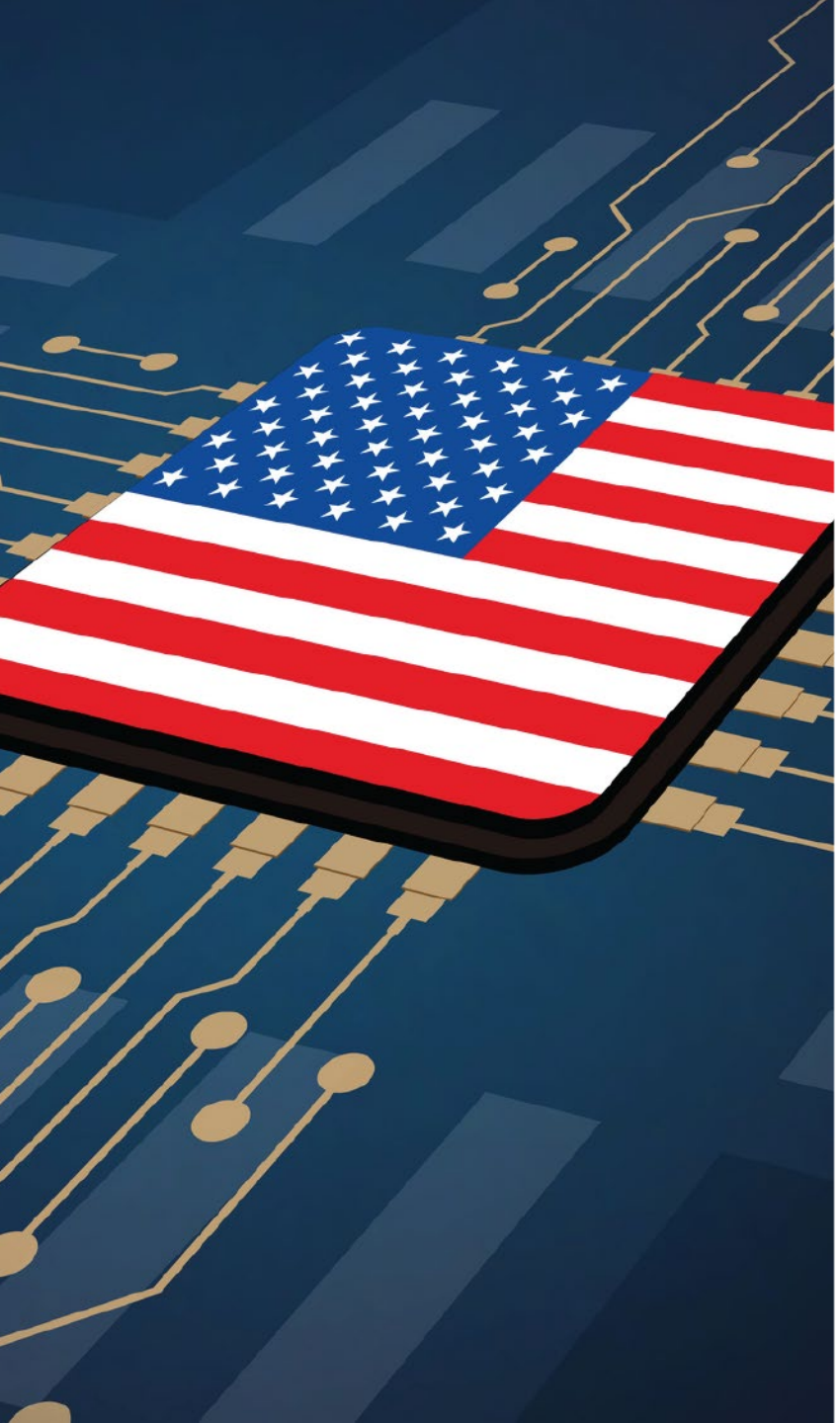
Day 3: March 8: Workforce, Supply Chain and Exhibitors Sessions

1. Technology and Manufacturing Workforce: Sampa Kochar, Tata, and Gokul Kumar, Micron
2. Supply Chain Session: Dr. Venky Sundaram and Kuldip Johal
3. Exhibitors Session: Ram Trichur and Ravi Bhaktal

12 SRAs, Faculty Leads & Institutions

1. Systems Design & Architecture	Prof. Binod Kumar, IITJ
2. Devices CMOS Power Si Photonics	 Profs. Abhisek Dixit, IITD & Nihar Marhotra, IITGN Profs. Satyam, IITBBS Prof Ankush, IITG Prof. Bijoy Das, IITM
3. Interconnecting Substrate- M&P	Prof. Pradeep Dixit, IITB
4. Interconnecting Substrate-Photonic	Naresh Emani, IITH, Shiv Govind, IITH Sudharsanan Srinivasan, IITM
5. Predictive Modeling & Design	Prof. Tarun Agarwal, IITGN
6. 6G Devices & Packaging	Prof. Mrinal Kanti Mandal, IITKGP
7. Integrated MEMS & Sensors	Prof. Bhaskar Mitra, IITD, Prof. Venkatesh, BITS Pilani
8. Materials for Devices & Packaging	Prof. Bhagawati Prasad, Prof. Praveen Ramamurthy, IISc
9. IC & Board Assembly & Reliability	Prof. Nilesh Badwe, IITK, Prof. Shiv Govind, IITH
10. Integrated Power Electronics	Prof. Shiladri Chakraborty, IITB
11.Thermal Designs & Technologies	Prof. Anandroop Bhattacharya, IITKGP
12. System Level Electrical Test	Prof. Jaynarayan Tudu, IITTP

https://www.ispec2025.in
Registration by invitation or contact@ispec2025.in



CHIPS R&D Office

International Opportunities and U.S. Engagement

CHIPS for America

$39 billion
for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

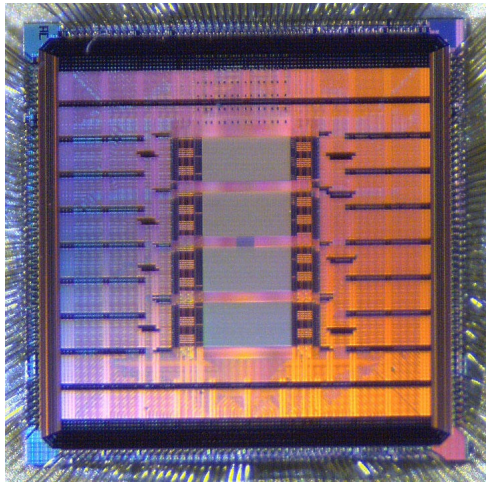
$11 billion
for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury

CHIPS R&D Goals



U.S. Technology Leadership

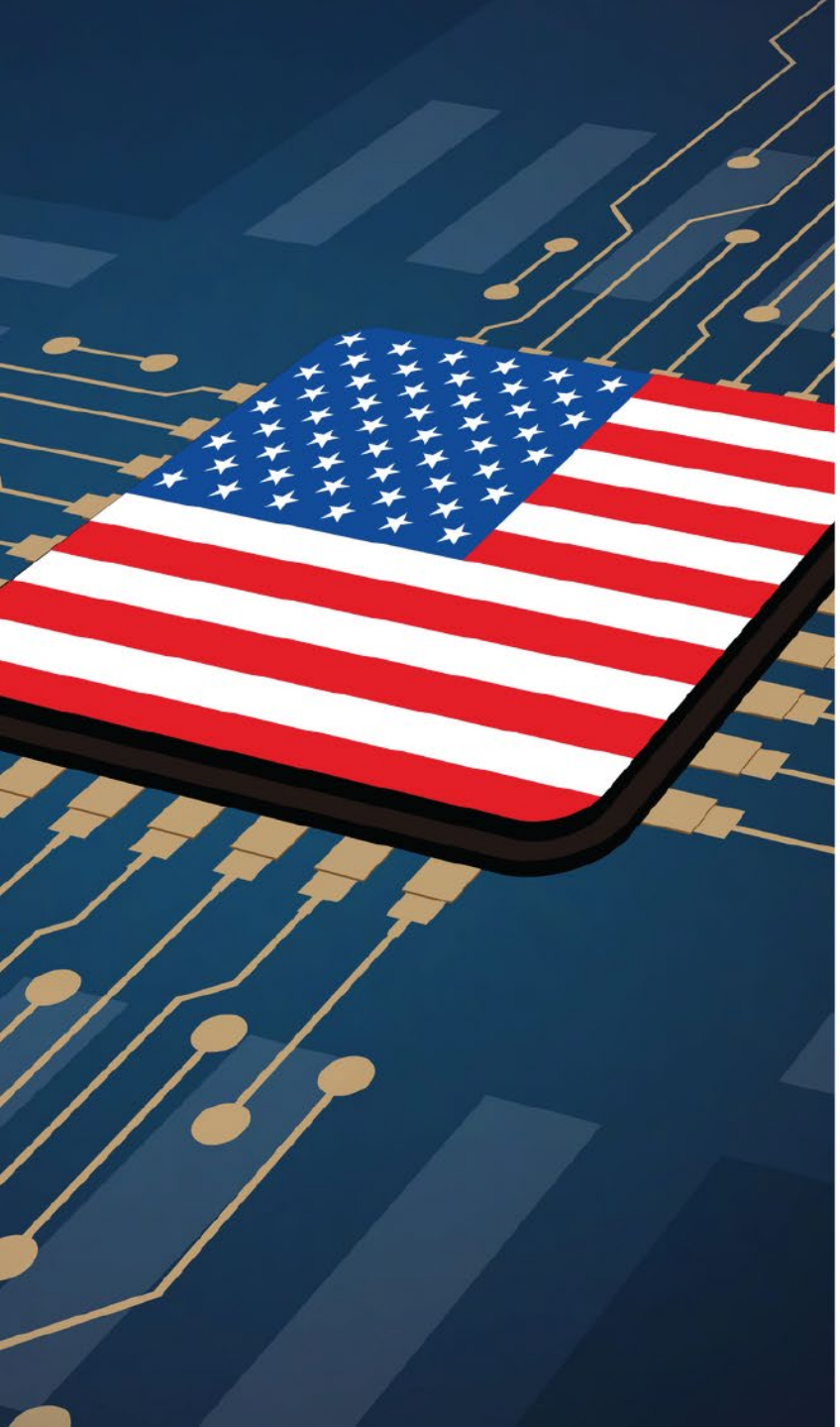
The United States establishes the capacity to invent, develop, prototype, and deploy the foundational semiconductor technologies of the future.

Accelerated Ideas to Market

The best ideas achieve commercial scale as quickly and cost effectively as possible.

Robust Semiconductor Workforce

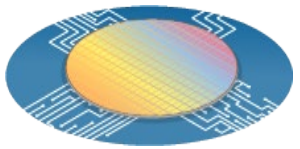
Inventors, designers, researchers, developers, engineers, technicians, and staff meet evolving domestic government and commercial-sector needs.



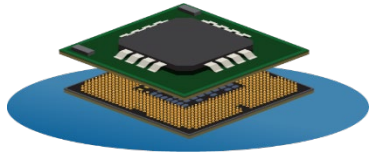
CHIPS for America R&D Programs

Manufacturing USA

Metrology



National Advanced Packaging Manufacturing Program

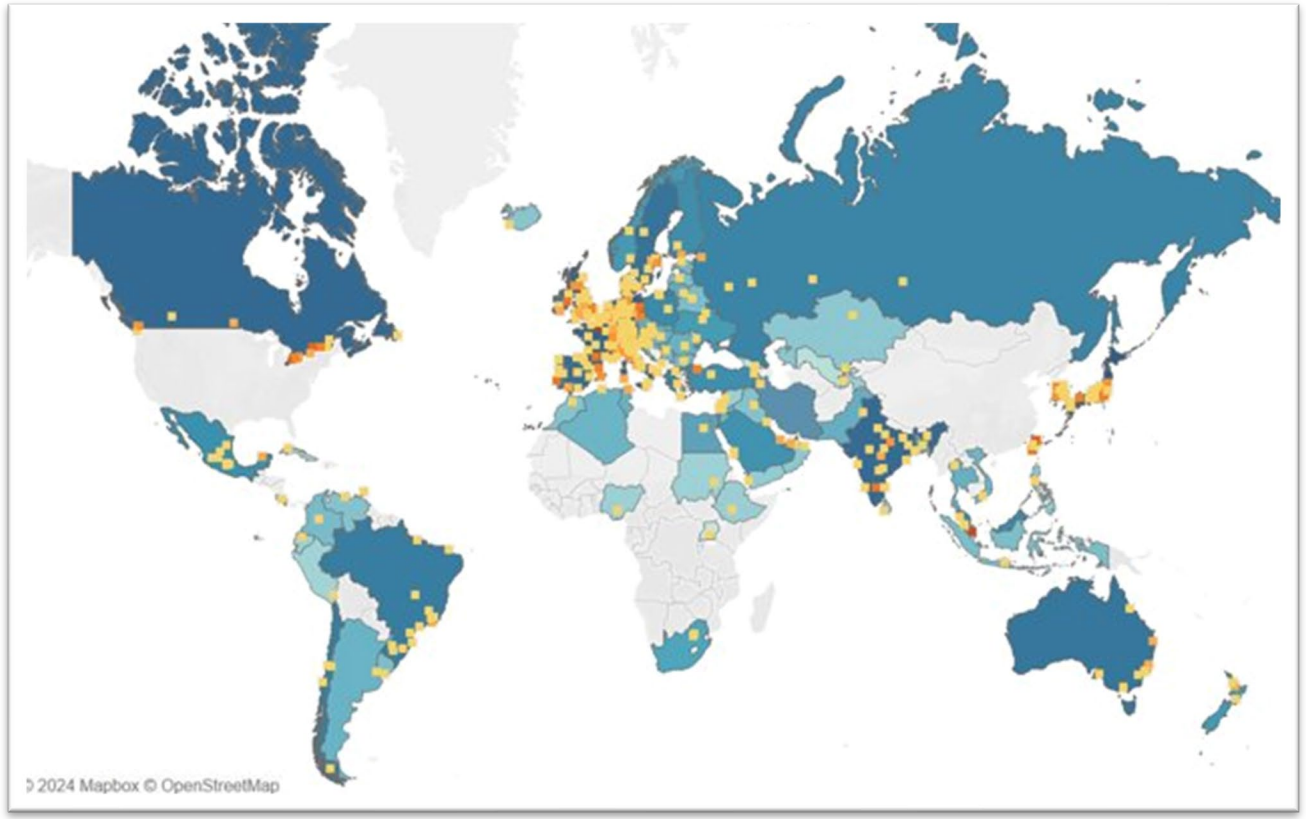


National Semiconductor Technology Center

Natcast

R&D International Landscape

- Semiconductor R&D, also a supply chain, spans the globe
- International cooperation can advance specific goals, expand infrastructure access, and drive work on shared challenges
- Expanding and emerging innovation clusters (Hsinchu, Paris, Seoul, Singapore, Tokyo, others)
- How can we best connect and leverage strengths across the globe?



*Global semiconductor R&D map drawn from R&D patent filings and published research from 2000-2024 outside U.S. and China

U.S. Engagement with International Partners

U.S.-led International Dialogues on Semiconductors

Americas

- Canada
- Costa Rica
- Mexico
- Uruguay

East Asia

- Japan
- Korea
- Malaysia
- Singapore
- Taiwan

Europe

- Netherlands
- United Kingdom

Multilateral

- G7
- EU

South Asia

- India

Supporting U.S. Initiatives

CHIPS for America

- R&D Office and Program Office staff leading international engagement in support of $50 billion in U.S. programs

International Technology and Security Innovation (ITSI) Fund

- $500 million over five years under U.S. Department of State for international engagement

Korea's Industry-Government Co-Investments for the Development of the Semiconductor Industry

Dr. Kwang-Seong Choi

Director and Research Fellow

ETRI, Korea

Korean Chips Act, March 2023

Purpose

Greater tax breaks for investments in the semiconductor industry.

Contents

Raises the corporate tax break for facility investment in the semiconductor and other strategic industries to 15 percent for large corporations such as Samsung Electronics and SK hynix, from the previous 8 percent.

The tax deduction rate for small- and mid-sized enterprises rose to 25 percent from 16 percent.

With the latest amendment including a new provision offering an additional 10 percent tax deduction on the increments in investment, conglomerates and companies could receive a tax cut of 25 percent at maximum.

Expected Effect

South Korea's top 10 chipmakers would save up to 360 billion won ($277 million) if the tax deduction rate is increased by 1 percentage point..

Semiconductor Specialized Complex, July 2023

Semiconductor Specialized Complex to offer a package of incentives for private investment in a bid to nurture the advanced sectors as a future semiconductor growth engine.

Yongin and Pyeongtaek

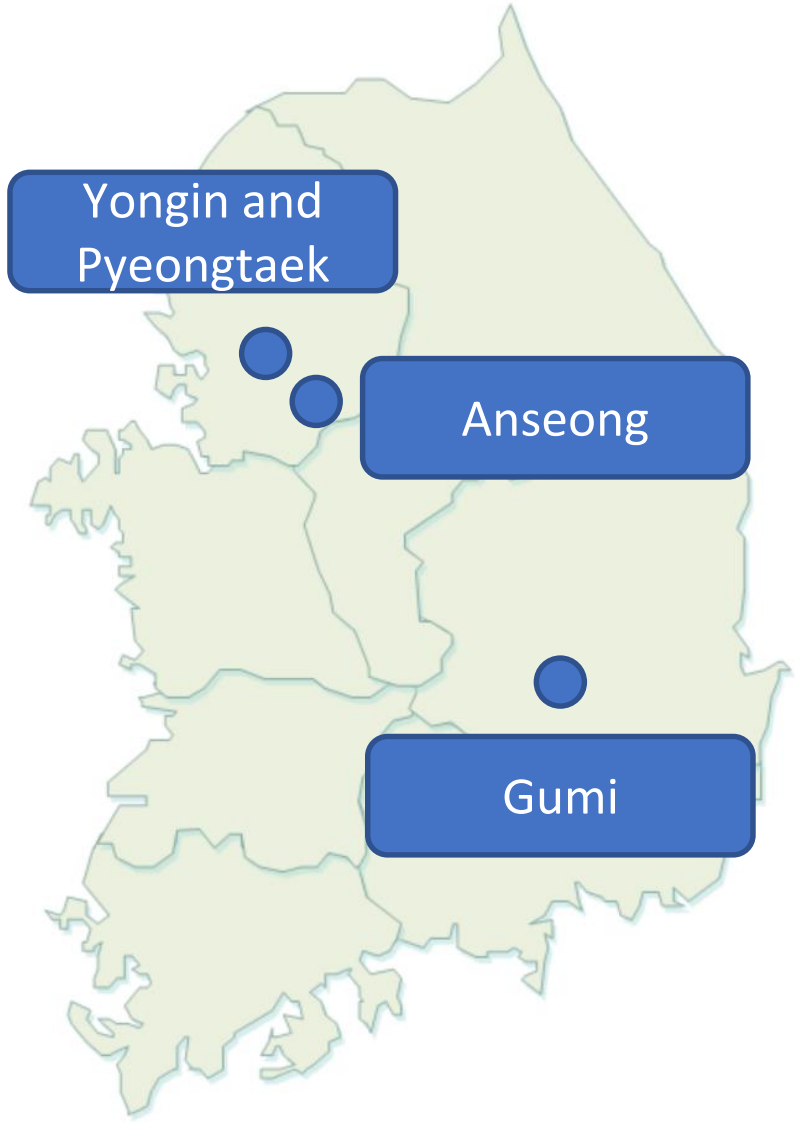
To support 56.2 billion won of investment in memory and system semiconductors by Samsung Electronics Co., SK hynix Inc. and other chipmakers by 2042

Gumi

SK Siltron Co., LG Innotek Co. and other firms plan to make an investment worth 4.7 trillion won combined by 2026

Anseong

Industrial zone for material, part and equipment businesses



Semiconductor Mega Cluster, January 2024

(Samsung Electronics) Yongin System Semiconductor Cluster (~’47)

Samsung Electronics Co. plans to invest a total of 500 trillion won for the project, including the 360 trillion-won budget for six new fabs in Yongin, 33 kilometers south of Seoul.

The country's top chipmaker will also invest 120 trillion won to build three new fabs in Pyeongtaek, 54 kilometers south of Seoul, along with three research fabs in Giheung with 20 trillion won.

(SK Hynix) Yongin Semiconductor Cluster (~'27)

No. 2 chipmaker SK hynix will allocate 122 trillion won to build four new fabs in Yongin

The ministry added the 622 trillion-won project will eventually create 3.46 million jobs during the process.

South Korea will take up 10 percent of the global market for non-memory chips by 2030 as well, rising sharply from the current estimate of 3 percent.

R&D Projects

South Korean news media outlet The Elec cited sources from the Ministry of Trade, Industry and Energy (MOTIE) and the Korea Evaluation Institute of Industrial Technology as indicating that the "Semiconductor Advanced Packaging Leading Core Technology Development Project" will cost between KRW300–500 billion (US$234–390.6 million) over a period of 5–7 years. The planning process is being helmed by Park Yong-chul, former CEO of Amkor Korea, who has chaired the promotion committee for the project.

As to the lead type, it will concentrate on technology segments where South Korean companies have demonstrated prowess, such as 2.5D package-based high-bandwidth memory (HBM) optimization, 10 to 40 micrometer (μm) bonding, and hybrid bonding, with the latter being particularly high profile lately, especially in the context of Nvidia's H100 AI GPU.

Source: Digitimesasia, Friday 4 August 2023

Thank you!